1. SYSTEM OVERVIEW

1.1 Overview

The D10P is a set of GNSS dual-band high-precision RTK navigation and positioning module which is based on the state of art CYNOSURE IV dual-core SoC chip. It is capable of tracking all global civil navigation systems (BDS, GPS, GLONASS, Galileo, QZSS, NavIC, and SBAS), as well as BDS-3 signals.

The latest dual-core architecture CYNOSURE IV adopts 22 nm process, with built-in dual-core MCU and 8Mbit MRAM, integrating multi-band multi-system GNSS RF and baseband. This newly designed architecture makes the module achieve centimeter level position accuracy and higher sensitivity, greater for improved jam resistance and multipath, and provide a highly robust service in complicated environment.

Along with its preeminent performance, the compact size (16.0×12.2×2.4 mm) of D10P of LCC package with lower consumption makes it suitable for various demands under different conditions. It can be widely used in mower, smart driving, surveying and mapping, unmanned aerial vehicles (UAVs), intelligent agriculture, and other fields.

1.2 Product Photo

1.3 Features

- Concurrent reception of multi-band multi-system satellite signals
- Tracking 128 GNSS signal channels at the same time
- Support BDS-3 signals: B1C, B2a
- Support PPP-B2b/PPP/PPP-RTK (upon request)
- Internal PVT, RTD, and RTK Engine
- Update rate up to 10 Hz
- Support A-GNSS
- Smart jammer detection and suppression
- Support four kinds of low power mode

GNSS reception

Mode	GPS/QZSS					BDS						GLONASS		Galileo				NavIC	SBAS
	L1CA	L1C	L2C	L5	L6	B1I	B1C	B2I	B2b	B2a	B3I	G1	G2	E1	E5a	E5b	E6	L5	L1
A (default)	●	*[1]	--	●	--	●	●	--	--	●	--	●	--	●	●	--	--	*[1]	●
B	●	*[1]	●	--	--	●	●	●	--	--	--	●	●	●	--	●	--	--	●
C	●	●	●	--	--	●	●	--	--	--	--	●	--	●	--	--	--	--	●

*[1] Supported upon request with special firmware

1.4 Block Diagram

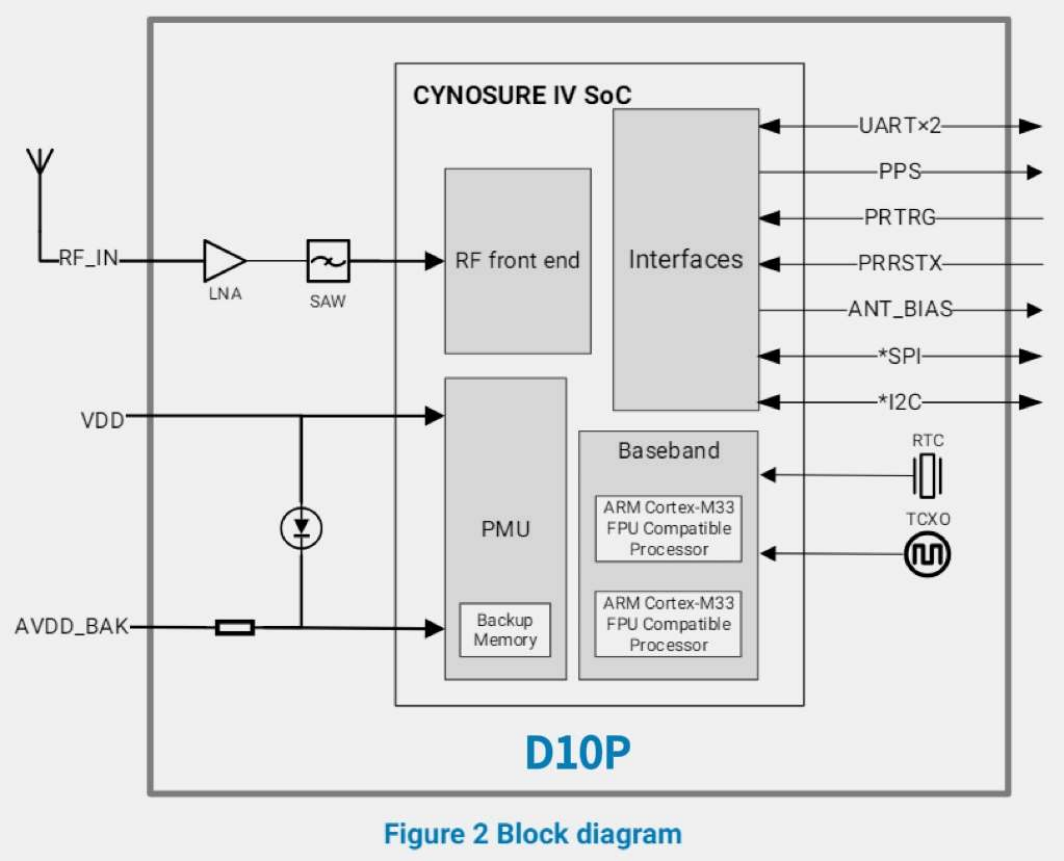

Figure 2 Block diagram

1.5 Specifications

Table 3: Specification

Parameter	Specifications		
Constellations	BDS, GPS, QZSS, GLONASS, Galileo, NavIC, SBAS		
Update rates	10Hz		
Position accuracy	GNSS		1.0m CEP
	SBAS		< 1.0m CEP
	RTK		1.0 cm + 1 ppm (H) 2.0 cm + 1 ppm (V)
Velocity & Time accuracy	GNSS		0.05 m/s CEP
	1PPS		20ns RMS
TTFF	Hot start		1s
	Cold start		27s
RTK	Convergence time		<10s
	Reliability		> 99.9%
Sensitivity[1]	Cold start		-148 dBm
	Hot start		-155 dBm
	Reacquisition		-158 dBm
	Tracking & navigation		-165 dBm
Protocol	NMEA-0183		
	RTCM 3.X		
Baudrate	230400 bps, by default		
Operating condition	Main supply		1.75V to 3.63V
	Digital I/O supply		1.75V to 3.63V
	Backup supply		1.62V to 3.63V
Power consumption	Tracking	GNSS	30 mA @ 3.3V
		Single system	18 mA @ 3.3V
	Standby	Data backup	16 uA
		RTC	1.4 uA
Serial interface	UART		2
	SPI[2]		1
	I2C[2]		1
Operating limit	Velocity		515 m/s
	Altitude		18,000m
Environmental conditions	Operating temp.		-40°C to +85°C
	Storage temp.		-40°C to +90°C
	Humidity		95% RH
Size	16.0×12.2×2.4 mm, 24pin LCC		

**[1] Demonstrated with a good external LNA*

**[2] Supported upon request with special firmware*

2 PIN DESCRIPTION

2.1 Pin Assignment

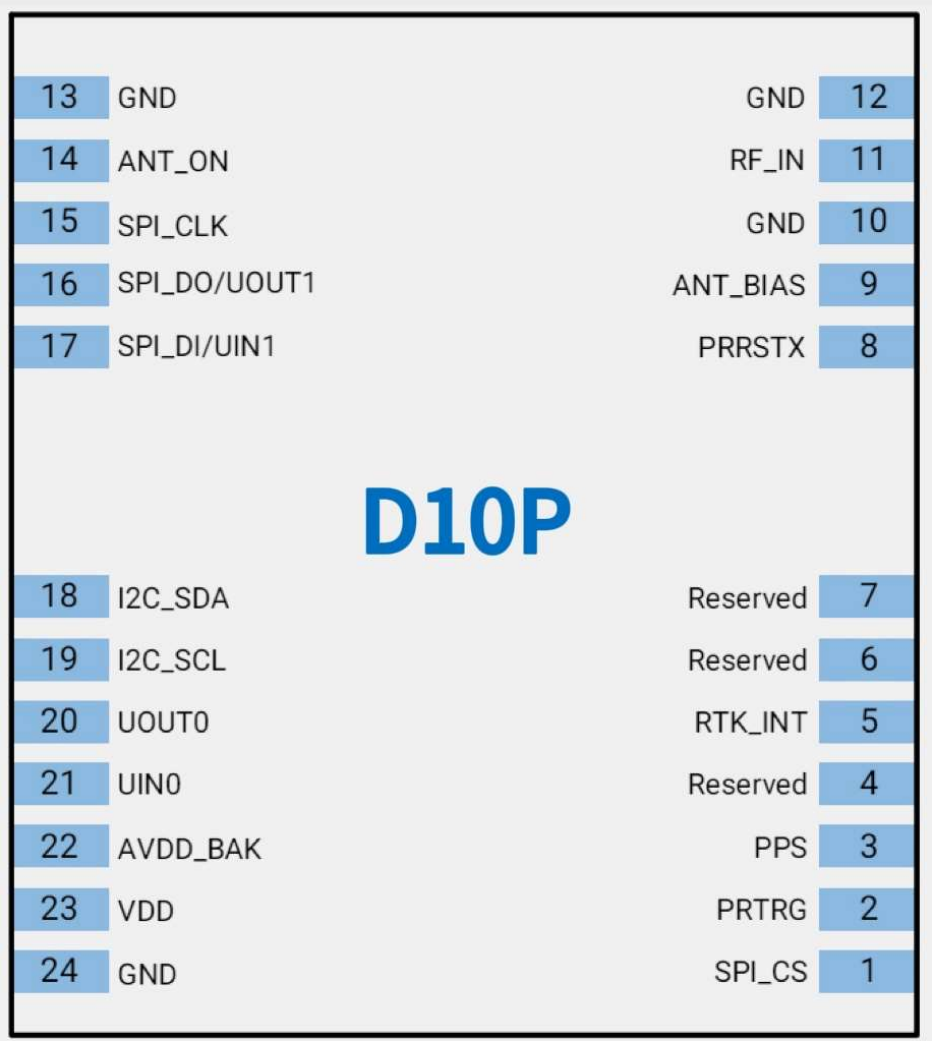

Figure 3 Pin assignment (top view)

2.2 Detailed Pin Descriptions

Table 4 Detailed pin descriptions

Function	Symbol	No.	I/O	Description
Power	GND	10,12, 13,24	G	Ground
	VDD	23	P	Main supply input.
	AVDD_BAK	22	P	Backup supply input.
Antenna	ANT_BIAS	9	O	RF section output voltage. Used to power the external active antenna. Leave it floating if not used.
	RF_IN	11	I	RF signal input.
	ANT_ON	14	O	External active antenna ON/OFF. Leave it floating if not used.
SPI [1]	SPI_CS	1	I/O	SPI interface. Leave it floating if not used.
	SPI_CLK	15	I	SPI clock. Leave it floating if not used.
	SPI_DO/UOUT1	16	O	SPI data output, or UART1 serial data output. Default as UART1. Leave it floating if not used.
	SPI_DI/UIN1	17	I	SPI data input, or UART1 serial data input. Default as UART1. Leave it floating if not used.
I2C [1]	I2C_SDA	18	I/O	I2C data. Leave it floating if not used.
	I2C_SCL	19	I/O	I2C clock. Leave it floating if not used.
UART	UOUTO	20	O	UART0 serial data output.
	UINO	21	I	UART0 serial data input.
Others	RTK_INT	5	O	RTK status output. Leave it floating if not used.
	PRRSTX	8	I	External reset, low active. Connect PRRSTX to the MCU during design. To meet the power on/off sequence control, do not leave this pin floating.
	PRTRG	2	I	Mode selection, or the trigger input to wake up the system.
	PPS	3	O	Time pulse output (PPS). Leave it floating if not used.
	Reserved	4,6,7	--	Reserved pin. Leave it floating.

*[1] Supported upon request with special firmware

3. ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Rating

Table 5 Absolute rating

Symbol	Parameter	Min.	Max.	Unit
VDD	Power input for the main power domain	-0.5	3.63	V
AVDD_BAK	Power input for the backup power domain	-0.5	3.63	V
VI max	Voltage input of I/O pin	-0.5	3.63	V
T env	Operation temperature	-40	85	℃
T storage	Storage temperature	-40	90	℃
T solder	Solder reflow temperature	--	260	℃

3.2 DC Characteristics

Table 6 DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power input for the main power domain	1.75	3.3	3.63	V
AVDD_BAK	Power input for the backup power domain	1.62	3.3	3.63	V
I ANT_BIAS	ANT_BIAS output current	--	--	25	mA
V ANT_BIAS	ANT_BIAS output voltage	--	VDD-0.2	--	V

3.3 ESD

Please add appropriate ESD protection on the module during design to ensure its functionality according to its application field.

Table 7 ESD protection performance

Pin	Contact discharge	Air discharge	Condition
RF_IN	±2kV	±4kV	HBM, 45% RH, 25℃
GND	±2kV	±4kV	
Others	±2kV	±4kV	

4. HARDWARE DESCRIPTION

4.1 Connecting Power

The module has two power supply pins: VDD and AVDD_BAK. The main power is supplied through the VDD pin, and the backup power is supplied through the AVDD_BAK pin. In order to ensure the positioning performance, please control the ripple of the module power supply as possible. It is recommended to use the LDO of a current above 200 mA, and PSRR not less than 70 dB for power supply. Add a magnetic bead on VDD pin if the power noise is high.

If the power for VDD pin is off, the real-time clock (RTC) and battery backed RAM (BBR) are supplied through the AVDD_BAK pin. Thus, orbit information and time can be maintained and will allow a Hot or Warm start. If no backup battery is connected, the module will perform a cold start at every power-up if no aiding data are sent to the module.

Note: If no backup supply is available, connect AVDD_BAK pin to VDD.

4.2 Power on/off Sequence

A permanent damage may occur with inappropriate power on sequence. So, please follow the rules below during design. To meet the requirement of controlling the power on/off sequence of the module, please connect the external reset pin (PRRSTX) to the MCU. Or, use a reset IC to control the sequence. It is recommended to adopt a low active, open-drain IC with 2.63V reset voltage threshold (APX803-26, SGM803B-RX, and UM803RS are preferred).

When both backup and main supply power on from their off state, external reset (PRRSTX) must be active and hold more than 5 ms after both backup supply and main supply reach the minimum operating voltage. The system power on sequence is illustrated in Figure 4 System power on sequence .

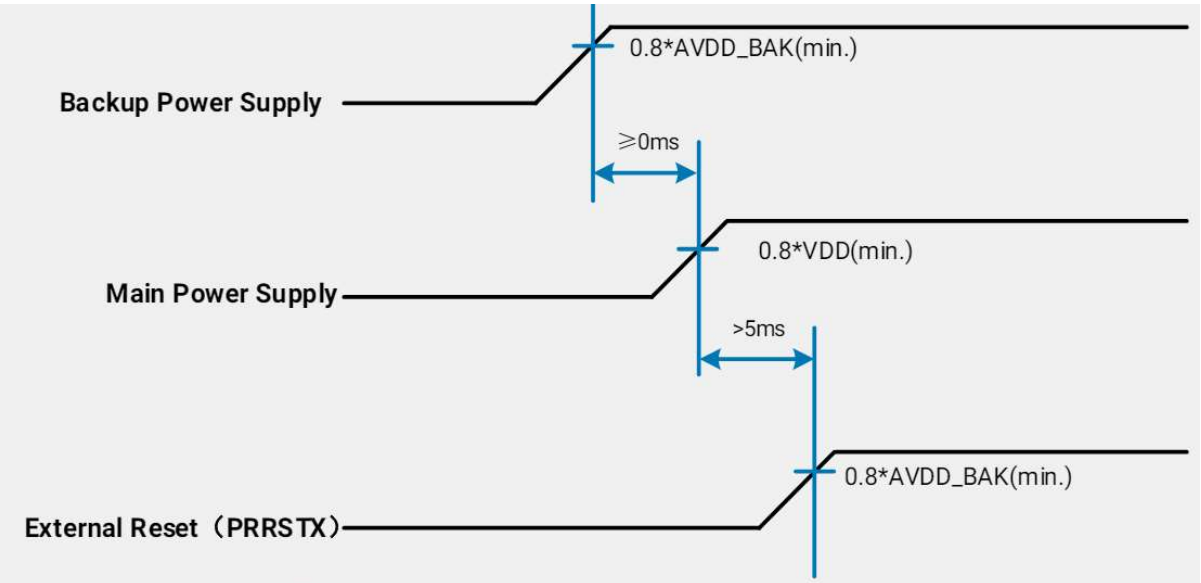

Figure 4 System power on sequence

4.3 Antenna Design

There is a built-in LNA and SAW in the module. It is recommended to use an active antenna with gain less than 30 dB and the noise figure less than 1.5 dB.

4.3.1 ANT_BIAS

The module has built-in short circuit detection and open circuit detection function, which can detect the status of normal connection, and send out antenna status prompt message in NMEA data.

- **Short circuit protection**
  » The module provides short circuit detection and protection functions for the antenna. Once an overcurrent is detected at the ANT_BIAS port, the module will restrict current output automatically to protect it from damages.
- **Open circuit detection**
  » The module can detect an open circuit in the antenna. Users can judge it from antenna status messages.

If an external power supply is used to power the antenna or a passive antenna is used, the antenna detection function will not work.

4.4 Reset and mode control

The operation mode of GNSS module is controlled by PRRSTX and PRTRG pin. While the module works in normal operation, keep PRRSTX and PRTRG pins at high level. The module will enter reset state when PRRSTX being low level (see Figure 6 Reset Timing). Operate PRTRG

and PRRSTX pins as the following instructions to enter **BootROM Command Mode** to update firmware. Please be aware that UART1 cannot be used for firmware upgrade.

- Keep PRTRG pin floating during system power-up or the external reset (PRRSTX from low to high), and the module will enter **User Normal Mode.**
- Drive PRTRG pin to low or connect PRTRG to GND directly (not by pull-down resistance) during system power-up or the external reset (PRRSTX from low to high), and the system enters **BootROM Command Mode** at PRTRG pin being released from low to floating state, and ready for firmware upgrading command.

When connecting PRRSTX and PRTRG to any host IO, DO NOT use the pull-up or pull-down resistance.

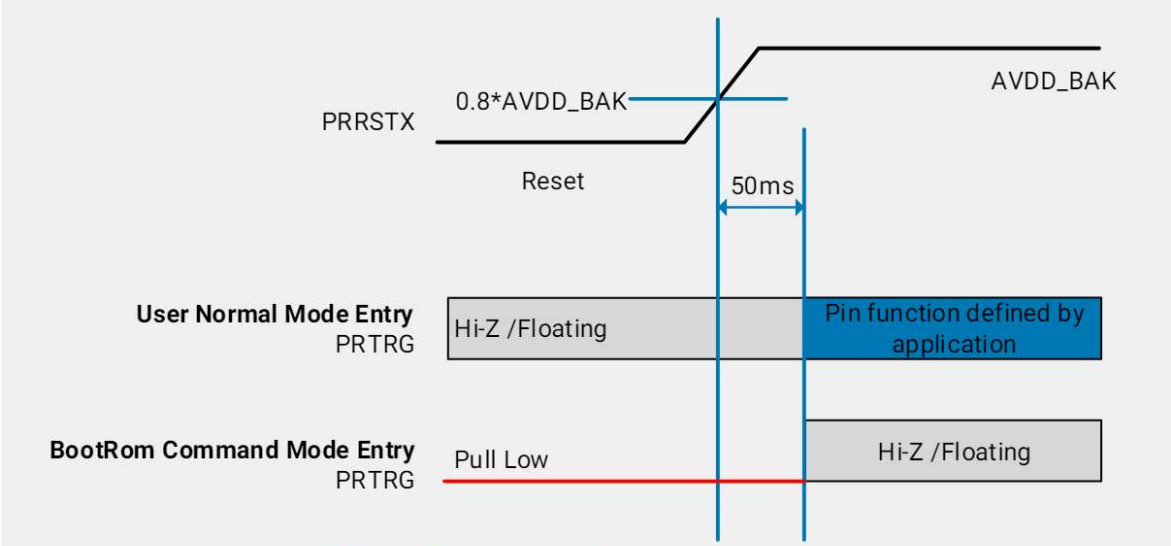

Figure 5 Switching the operation mode

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Reset Timing	t_{RSTL}	PRRSTX	Connected to a stable power source, and TCXO clock remains stable.	100	--	--	mS

Figure 6 Reset Timing

5 MECHANICAL SPECIFICATION

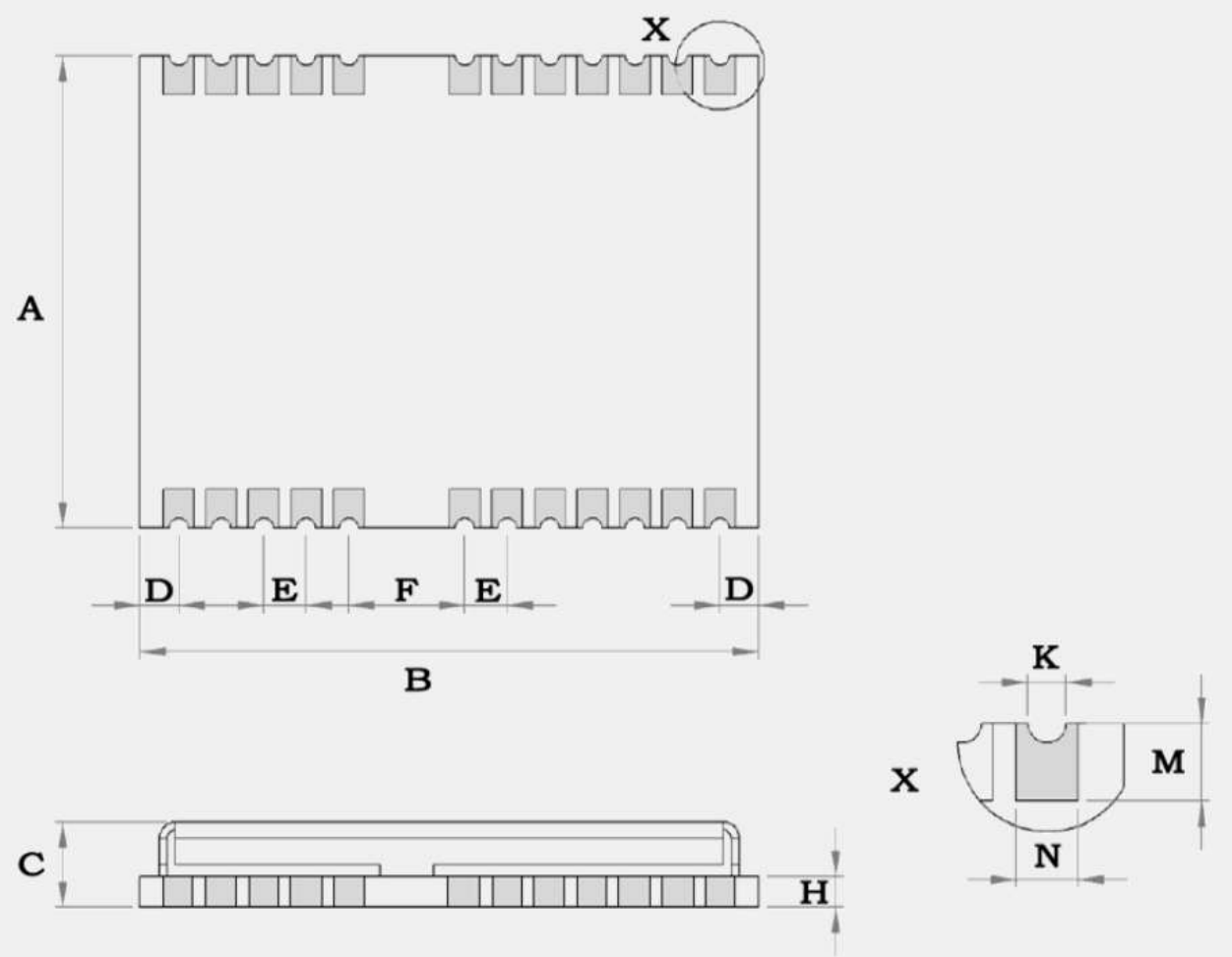

Figure 7 Dimensions

Table 9 Dimensions

Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	12.0	12.2	12.4
B	15.8	16.0	16.2
C	2.2	2.4	2.6
D	0.9	1.0	1.3
E	1.0	1.1	1.2
F	2.9	3.0	3.1
H	--	0.8	--
K	0.4	0.5	0.6
M	0.8	0.9	1.0
N	0.7	0.8	0.9

6 REFERENCE DESIGN

6.1 Reference Design

This section provides a full elaboration for the reference design of D10P modules. For more detailed information, please refer to *Hardware Application Guide for GNSS Modules.*

Please follow these instructions during hardware design:

1) A 27-39 nH inductor is used only when an active antenna is connected, and no need for a passive antenna. The active antenna is preferred to ensure the positioning performance.

2) The antenna detection is achieved through detecting the ANT_BIAS current, whose maximum output value is 35 mA. An external power supply is required to power the antenna if the power consumption of the active antenna is greater than 35 mA. When using an external power supply or a passive antenna, the module cannot detect the antenna status, and the user needs to add a detection circuitry externally to perform antenna detection.

3) In the case of using an external power supply to power the antenna, it is recommended to use a 100 pF stopping capacitor to avoid the RF interface damage because of the inconsistent voltage.

4) A diode is used to connect the AVDD_BAK pin and VDD pin internally, which can charge the external backup battery. See 1.4 Block diagram for details.

5) Due to the strong drive capability of the UART pin, installing an RC circuit, instead of a pull-up resistance, can effectively prevent the UART signal from interfering with other signals.

6) Connect the PRRSTX pin to the MCU to control the power on/off sequence. Or, the module is likely to be damaged.

7) Connect the PRTRG pin to the MCU for upgrading. Or, the OTA upgrade will not function.

8) When connecting the PRRSTX and PRTRG to any MCU IO, adopt the IO pin with OD output function, and do not include any pull-up or pull-down resistance to the PRRSTX and PRTRG pin.

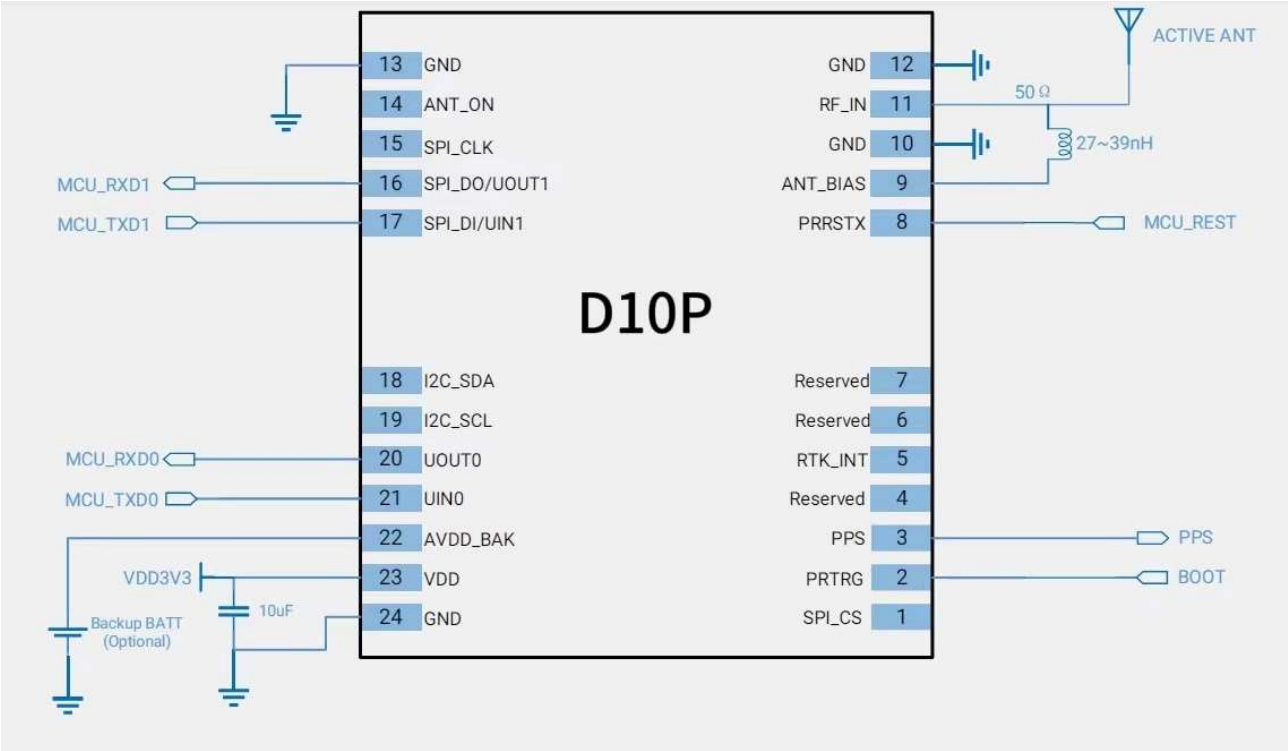

Figure 8 Reference design of active ant. supplied by ANT_BIAS

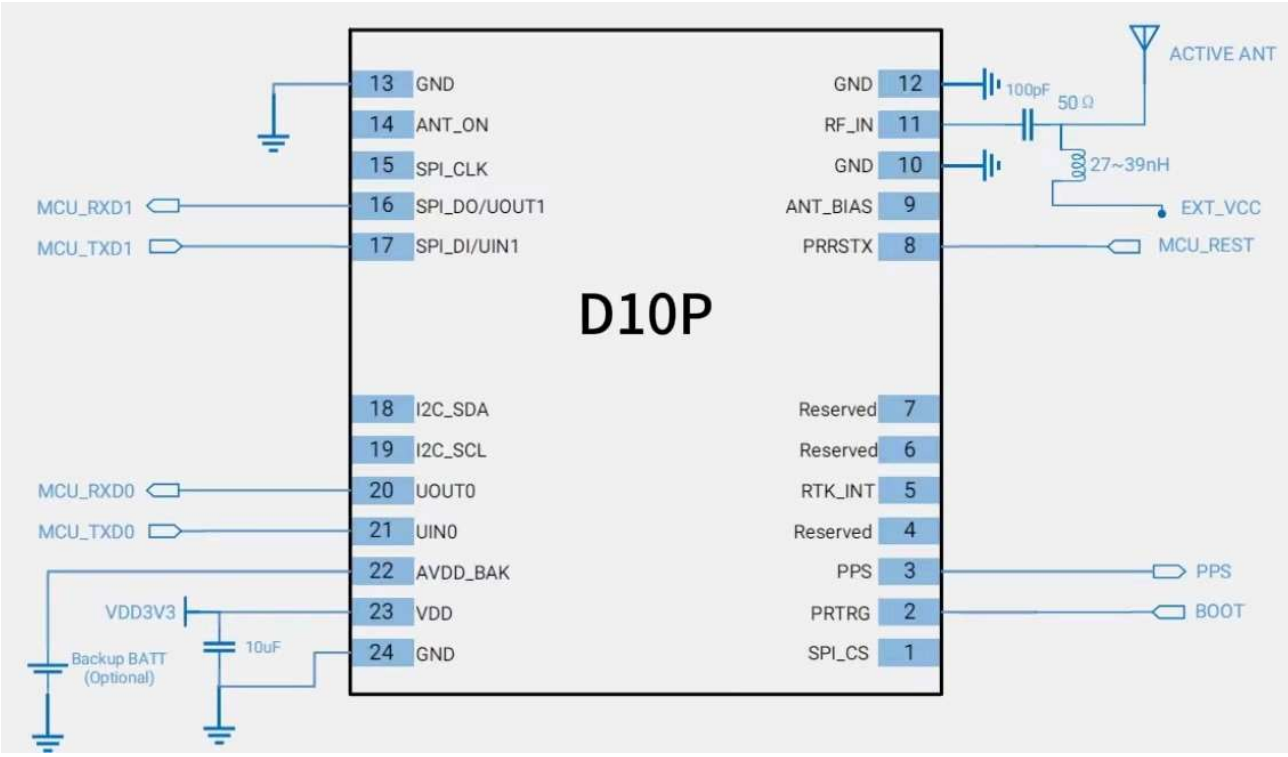

Figure 9 Reference design of active ant. supplied by external power

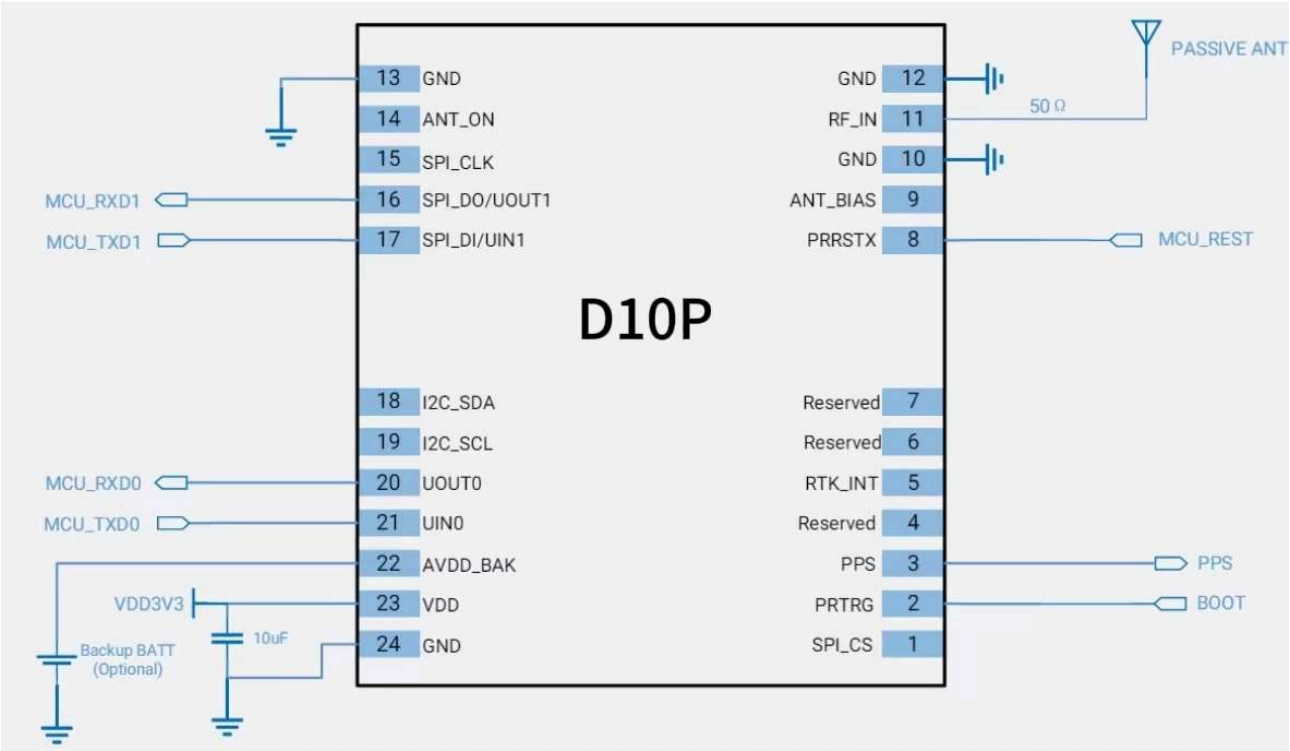

Figure 10 Reference design of passive ant.

6.2 PCB Footprint Reference

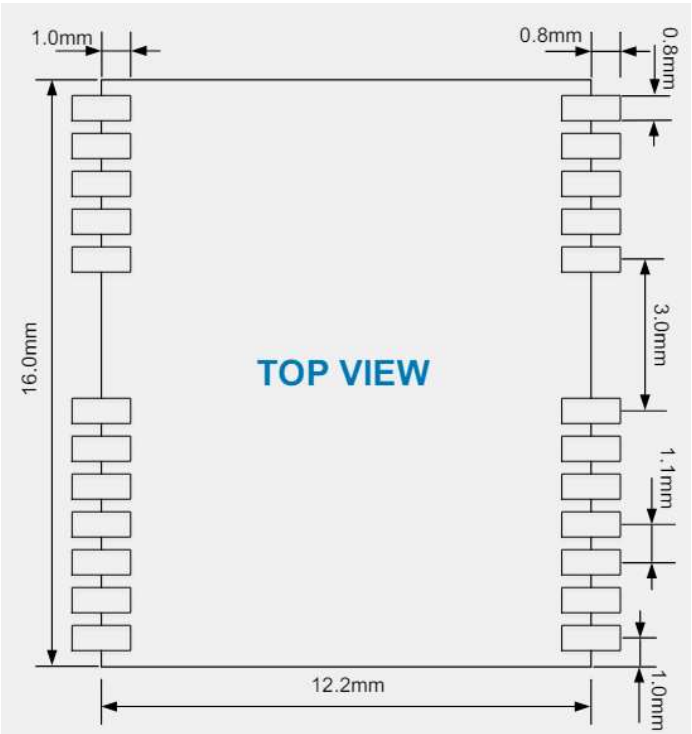

Figure 11 PCB Footprint Reference

6.3 Layout Notes

1) A decoupling capacitor should be placed close to VDD pin of the module, and the width of power routing should be more than 0.5 mm

2) The width of RF routing between RF port to antenna interface should be wider than 0.2 mm. The characteristic impedance of RF routing between RF port to antenna interface should be controlled to 50Ω.

3) It is recommended that the routing from RF port to antenna interface refers to the second layer, and no routing are recommended on the layer.

4) Do not place the module close to any EMI source, like antenna, RF routing, DC/DC or power conductor, clock signal or other high-frequency switching signal, etc.

7 DEFAULT MESSAGE

Interface	Settings
UART output	Data format: 8 data bits, no parity bit, 1 stop bit Default baud: 230400 bps Configured to transmit both NMEA and HD Binary protocols, but only the following NMEA (and no HD Binary sentence) messages have been activated at start-up: GGA, GSA, GSV, RMC, ZDA, TXT-ANT
UART input	Data format: 8 data bits, no parity bit, 1 stop bit Default baud: 230400 bps Default protocol: HD binary protocol, RTCM message.
PPS	1 pulse per second, synchronized at rising edge, pulse length 100 ms

* *Refer to GNSS_Protocol_Specification for information about other settings.*

The default configuration and output information of UART0 and UART1 are identical, among which UART1 cannot be used for firmware upgrade. If the UART is connected well to the MCU when VDD is off, a high UART level may cause residual power on VDD, leading to power on failure. Therefore, when VDD is off, it is advisable to disconnect the UART or set MCU_UART to the input or high resistance state.

8 PACKAGING INFORMATION

8.1 Packing

The module is a Moisture Sensitive Device (MSD) and Electrostatic Sensitive Device (ESD). During packing and shipping, it is strictly required to take appropriate MSD handling instructions and precautions. The table below shows the general packing hierarchy for the standard shipment.

Table 10 Packing hierarchy

Module	Reel	Sealed bag	Packing box	Shipping carton
				

8.1.1 Tape and Reel

D10P is delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down. The figure below shows the tape dimensions.

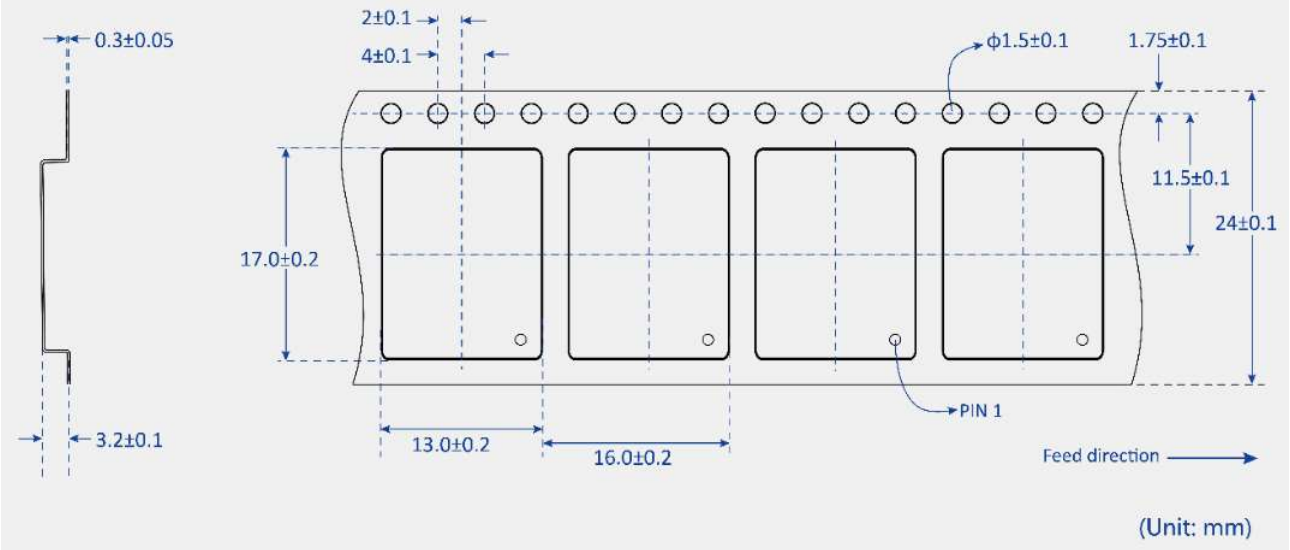

Figure 12 Tape dimensions

D10P is deliverable in quantities of 1000 pcs on a reel. The figure below shows the dimensions of the reel.

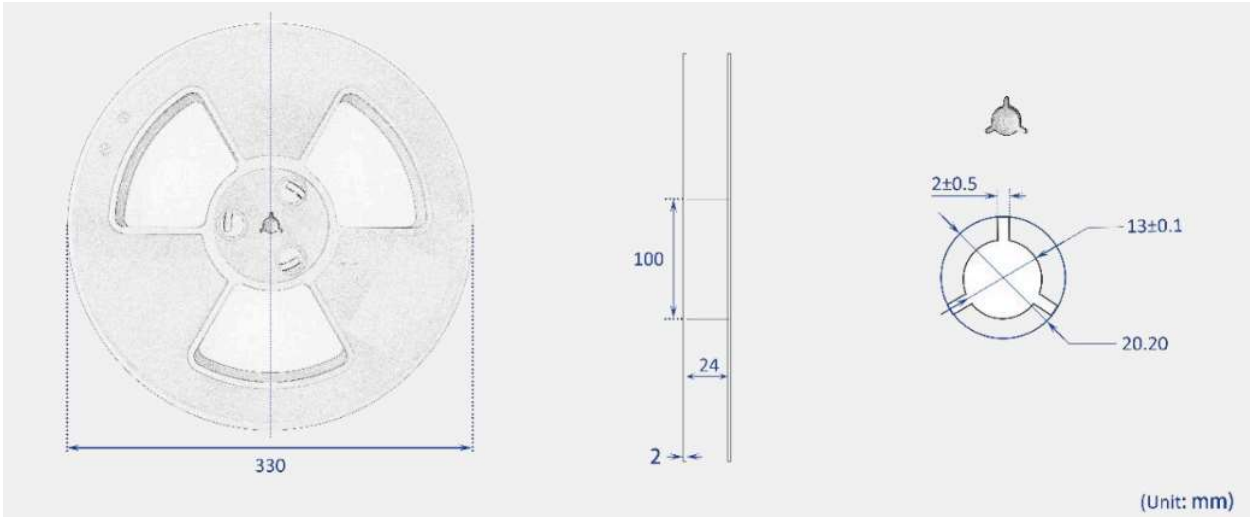

Figure 13 Reel dimensions

8.1.2 Shipment Packaging

The reels are packed in the sealed bags in a box and shipped by shipping cartons. Up to five boxes (1000 pcs in total) can be packed in one shipping carton.

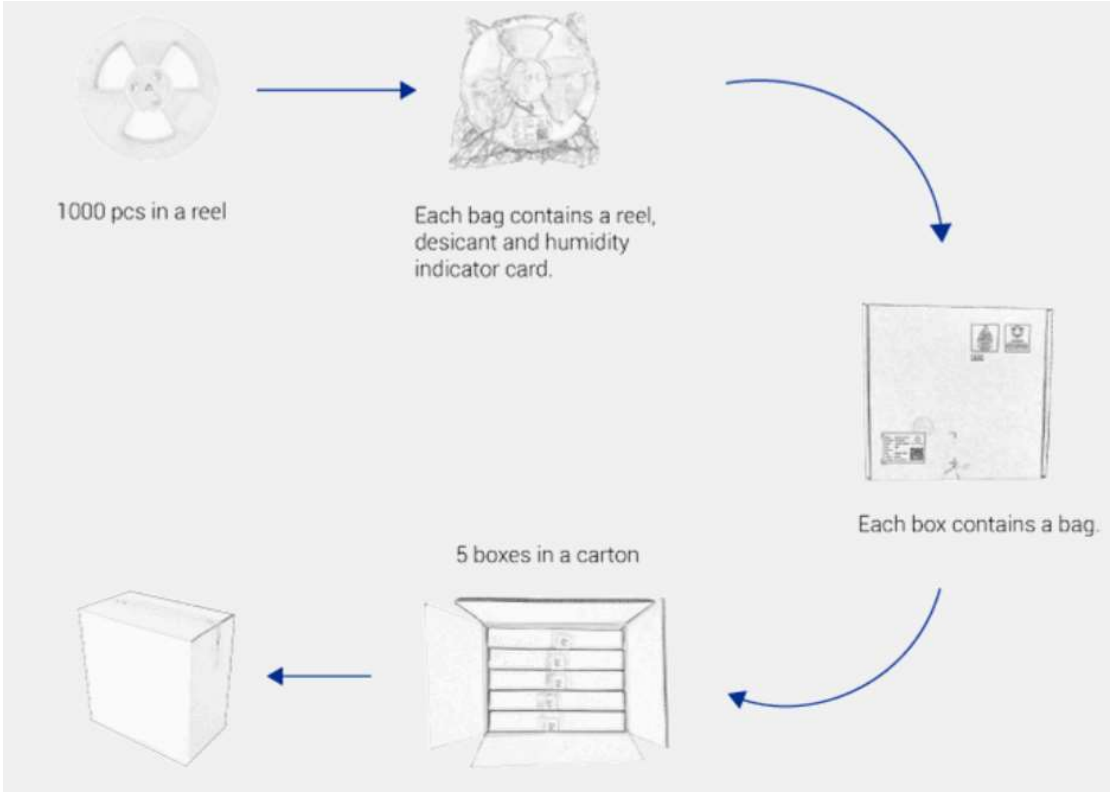

Figure 14 Packaging

8.2 Storage

In order to prevent moisture intake and protect against electrostatic discharge, D10P is packaged together with a humidity indicator card and desiccant to absorb humidity.

8.3 ESD Handling

8.3.1 ESD Handling Precautions

D10P which contains highly sensitive electronic circuitry is an Electrostatic Sensitive Device (ESD). Observe precautions for handling! Failure to observe these precautions may result in severe damage to the GNSS module!

- Unless there is a galvanic coupling between the local GND (i.e. the workbench) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10 pF, coax cable ~50 - 80 pF/m, soldering iron …)
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the module's RF pin, make sure to use an ESD safe soldering iron (tip).

8.3.2 ESD Protection Measures

The GNSS positioning module is sensitive to static electricity. Whenever handling the module, particular care must be exercised to reduce the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account.

- Adds ESD Diodes to the RF input part to prevent electrostatics discharge.
- Do not touch any exposed antenna area.
- Adds ESD Diodes to the UART interface

8.3.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) of the GNSS module is MSL3.